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EXAMINER	
LI, AIMEE J	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/737,342	MOORE ET AL.	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2000 and 22 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-54* is/are pending in the application.

4a) Of the above claim(s) *51-54* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-50 have been considered. Claims 51-54 have been withdrawn.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Drawings as filed on 26 march 2001 and IDS as filed on 22 August 2001.

Election/Restrictions

3. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-50, drawn to an operations manager, classified in class 712, subclass 201.

   II. Claims 51-54, drawn to the operation of specific Load and Store instructions, classified in class 712, subclass 225.

4. The inventions are distinct, each from the other because of the following reasons:

5. Inventions I and II are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because the operations manager is effective for all types of instructions, not necessarily only Load and Store instructions. The subcombination has separate utility such as loading and storing data in other devices, which do not use the operations manager described.

6. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

7. During a telephone conversation with Richard F. Frankeny (Reg. No. 47,573) on 02 March 2004 a provisional election was made without traverse to prosecute the invention of Group I, claim1-50. Affirmation of this election must be made by applicant in replying to this Office action. Claims 51-54 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

8. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Drawings

9. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the apparatus of claim 1, specifically the plurality of addressable registers, first comparison circuit, second comparison circuit, and dispatch circuit, and data processing system of claim 26, specifically the plurality of addressable registers, first comparison circuit, second comparison circuit, and dispatch circuit, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

10. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

11. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "203" on page 8, line 1 has been used to designate both the TLB in the IMU and the TLB in the SMU. It is unclear whether these are the same TLB or separate TLBs. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

12. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "911" has been used to designate both the operand mask on page 13, lines 13 and 16 and a portion of the Quadword in figure 9. It is unclear what the specification is referring to in the figure. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

13. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "1010" has been used to designate both the Quadword operand in Figure 10 and the Operand Mask on page 14, line 1. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

14. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "1323" on page 33, lines 14-15 has been used to designate both a track ball

and a mouse. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

15. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "911" and "912" have both been used to designate a Quadword Operand. It is unclear the different between elements 911 and 912, since they are both labeled with "Quadword Operand". A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

16. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: page 33, lines 14, 15, and 17 element 1323 and page 33, line 18 element 1338. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

17. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: Figure 5, element 503; Figure 6, elements 600, 616, 617, 618, 619, and 620; Figure 7, element 704; Figure 8, element 807; Figure 9, elements 912 and 915; Figure 10, element 1011; Figure 12, element 1205; and Figure 13, elements 1326 and 1340. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

18. The abstract of the disclosure is objected to because page 48, line 7 reads "Load operations that *transfer of data* from the memory". Please correct to read --Load operations that *transfer data* from the memory--. The correction is highlighted in italics. Correction is required. See MPEP § 608.01(b).

19. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

20. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

21. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

22. Claims 1-50 has been rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The independent claims 1 and 25 recite the limitations a first comparison circuit, a second comparison circuit, and a dispatch circuit. The examiner could not locate in the specification a clear and concise description of an apparatus which includes the first and second comparison circuit sand dispatch circuit and operates them as described in the claim language. The specification has a high level

description of how Load and Store instructions operate with an SRB present, but there is no description of an apparatus with two comparison circuits and dispatch circuit nor is there description about how the apparatus uses the comparison circuits and dispatch circuit.

23. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

24. Claims 1-50 recite the limitations

a. A first comparison circuit, said first comparison circuit operable to scan and compare a value in a set of said data entry fields to a predetermined input value.

b. A second comparison circuit, said second comparison circuit operable to compare a first register address corresponding to a comparison match of said first comparison circuit to a second register address; and

c. A dispatch circuit operable to dispatch data of a second data entry field of a second register corresponding to said second register address to an operation unit in response to a decode of data in a third data entry field of said second register and a comparison match of said second comparison circuit.

25. There is insufficient antecedent basis for this limitation in the claim. There is insufficient basis in the specification for these claims.

Claim Rejections - 35 USC § 102

26. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

27. Claims 1-12 and 14-25 are rejected under 35 U.S.C. 102(b) as being taught by Tran et al., U.S. Patent Number 5,764,946 (herein referred to as Tran).

28. Referring to claim 1, Tran has taught an apparatus for managing operations in a processor (Tran column 6, line 52 to column 7, line 14), said apparatus comprising:

a. A plurality of addressable registers, each of said registers partitioned into plurality of data entry fields (Tran column 1, line 49 to column 2, line 25);

b. A first comparison circuit, said first comparison circuit operable to scan and compare a value in a set of said data entry fields to a predetermined input value (Tran column 77, lines 33-47; column 779, lines 24-55; column 80, line 5 to column 81, line3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; Figure 40 Figure 44; and Figure 46);

c. A second comparison circuit, said second comparison circuit operable to compare a first register address corresponding to a comparison match of said first comparison circuit to a second register address (Tran column 77, lines 33-47; column 779, lines 24-55; column 80, line 5 to column 81, line3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; Figure 40 Figure 44; and Figure 46); and

d. A dispatch circuit operable to dispatch data of a second data entry field of a second register corresponding to said second register address to an operation unit in response to a decode of data in a third data entry field of said second register and a comparison match of said second comparison circuit (Tran column 106, line 35 to column 107, line 62; Figure 48; and Figure 49).

29. Referring to claim 2, Tran has taught wherein said operations are Load and Store operations within said processor (Tran column 77, lines 33-47; column 779, lines 24-55; column 80, line 5 to column 81, line3; Figure 38; Figure 39; and Figure 40).

30. Referring to claim 3, Tran has taught wherein said predetermined input value is a real address requesting particular data corresponding to one of a Load and a Store operation (Tran column 77, lines 33-47; column 779, lines 24-55; column 80, line 5 to column 81, line3; Figure 38; Figure 39; and Figure 40).

31. Referring to claim 4, Tran has taught wherein said first scan comparison circuit comprises multiple like entry comparison circuits, each of said multiple like entry comparison circuits operable concurrently in parallel (Tran column 77, lines 33-47; column 779, lines 24-55; column 80, line 5 to column 81, line3; Figure 38; Figure 39; and Figure 40).

32. Referring to claim 5, Tran has taught wherein said operation unit comprises an Instruction Management Unit (IMU) (Trans column 6, line 52 to column 8, line 57 and Figure 1).

33. Referring to claim 6, Tran has taught wherein said operation unit comprises a Storage Management Unit (SMU) said SMU comprising data cache memory and controller and a Storage Reference Buffer (SRB) (Tran column 10, line 66 to column 11, line 15; column 77, lines 33-47; column 779, lines 24-55; column 80, line 5 to column 81, line3; Figure 1; Figure 38; Figure 39; and Figure 40).

34. Referring to claim 7, Tran has taught wherein one of said data entry fields is a Valid bit field, said Valid bit field indicating whether other data entry fields are valid (Applicant's claims 7 and 32) (Tran column 123, lines 2-15 and Figure 55).

35. Referring to claim 8, Tran has taught wherein one of said data entry fields is an Instruction Identification (ID) field corresponding to a particular Load and Store operation (Tran column 123, lines 2-15 and Figure 55).

36. Referring to claim 9, Tran has taught wherein one of said data entry fields is an Instruction status field corresponding to a status of one of said Load and Store operations (Tran column 123, lines 2-15 and Figure 55).

37. Referring to claim 10, Tran has taught wherein one of said data entry fields is a Load/Store field having a Load/Store bit, said Load/Store bit corresponding to a Load operation if said Load/Store bit has a first logic state and corresponding to a Store operation if said Load/Store bit has a second logic state (Tran column 123, lines 2-15 and Figure 55).

38. Referring to claim 11, Tran has taught wherein one of said data entry fields comprises Real Address field, said Real Address field corresponding to a particular Real Address of memory data (Tran column 123, lines 2-15 and Figure 55).

39. Referring to claim 12, Tran has taught wherein one of said data entry fields is a Quadword field, said Quadword field comprising multiple bytes of data (Tran column 123, lines 2-15 and Figure 55). In regards to Tran, he has taught the data is present in an entry field. The size of the field is not a patentable distinction.

40. Referring to claim 14, Tran has taught wherein said operation unit is a pipeline execution unit operating concurrently on a plurality of said data entry fields (Tran column 10, lines 17-55 and Figure 1).

41. Referring to claim 15, Tran has taught wherein said addressable registers are addressed using a plurality of address pointers (Tran column 77, lines 33-47; column 779, lines 24-55;

column 80, line 5 to column 81, line3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; Figure 40 Figure 44; and Figure 46).

42. Referring to claim 16, Tran has taught wherein said addressable registers are configured as a Storage Reference Buffer (SRB) (Tran column 10, line 66 to column 11, line 15; column 77, lines 33-47; column 779, lines 24-55; column 80, line 5 to column 81, line3; Figure 1; Figure 38; Figure 39; and Figure 40).

43. Referring to claim 17, Tran has taught wherein one of said address pointers is a third pointer, said third pointer pointing to one of said addressable registers whose data entry fields contain data defining an earliest Store operation that is either unresolved or that matches a register address of a current Load operation (Tran column 70, lines 7-44 and Figure 36).

44. Referring to claim 18, Tran has taught wherein said address pointers comprise a fourth and a fifth pointer, said fourth and fifth pointers defining a window of register addresses from which a Load operation may be satisfied without having to access other memory storage (Tran column 70, lines 7-44 and Figure 36).

45. Referring to claim 19, Tran has taught wherein said second register address is selected from registers addresses which fall within a window of register addresses, said window of addresses defined by said address pointers (Tran column 70, lines 7-44; column 81, lines 1-3; and Figure 36).

46. Referring to claim 20, Tran has taught wherein one of said address pointers is a first pointer, said first pointer pointing to an IN register address of a first available register into which data may be added (Tran column 70, lines 7-44 and Figure 36).

47. Referring to claim 21, Tran has taught wherein one of said address pointers is a second pointer, said second pointer pointing to an OUT register address of a first available register from which register data may be retired (Tran column 70, lines 7-44 and Figure 36).

48. Referring to claim 22, Tran has taught wherein said data entry fields, added to said SRB after a mis-predicted branch instruction occurs in said processor, are retired and said first pointer is indexed to first register address of a register with added register data entry bits which were added immediately prior to said mis-predicted branch instructions (Tran column 82, line 63 to column 83, line 22).

49. Referring to claim 23, Tran has taught wherein said window of register addresses defines active Load and Store operations (Applicant's claims 23 and 48) (Tran column 70, lines 7-44 and Figure 36).

50. Referring to claim 24, Tran has taught wherein said first pointer is indexed by one when said register data has been added, said first pointed having a minimum and a maximum value wherein a decrement down from a minimum value results in said maximum value and an increment up from said maximum value results in said minimum value (Tran column 70, lines 7-44 and Figure 36).

51. Referring to claim 25, Tran has taught wherein said second pointer is indexed by one when register entry bits have been deleted, said second pointer having a minimum and a maximum value wherein a decrement down from said minimum value results in said maximum value and an increment up from said maximum value results in said minimum value (Tran column 70, lines 7-44 and Figure 36).

Claim Rejections - 35 USC § 103

52. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

53. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tran et al., U.S. Patent Number 5,764,946 (herein referred to as Tran), as applied to claim 1 above, in view of Jerry M. Rosenberg's Dictionary of Computers, Information Processing & Telecommunications Second Edition ©1987 (herein referred to as Rosenberg). Tran has not explicitly taught wherein one of said data entry fields is an Operand Mask field, said Operand Mask field defining selected bytes of data within a selected one of said data entry fields. However, Tran has taught miscellaneous control fields (Tran column 123, lines 2-15 and Figure 55). Rosenberg has explicitly taught a mask field (Rosenberg page 370). A person of ordinary skill in the art would have recognized that a mask field describes certain data needed while ignoring unnecessary data, thereby ensuring the unnecessary data does not affect the system. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the mask field of Rosenberg in the device of Tran.

54. Claims 26-37 and 19-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tran et al., U.S. Patent Number 5,764,946 (herein referred to as Tran) in view of Kenneth L. Short's Microprocessors and Programmed Logic ©1981 (herein referred to as Short).

55. Referring to claim 26, Tran has taught a data processing system, comprising:

a. A central processing unit (CPU) (Tran column 6, lines 42-55);

b. Said CPU comprising an apparatus for managing operations in a processor (Tran column 6, line 52 to column 7, line 14), said apparatus comprising:

i. A plurality of addressable registers, each of said registers partitioned into a plurality of data entry fields (Tran column 1, line 49 to column 2, line 25);

ii. A first comparison circuit, said first comparison circuit operable to scan and compare a value in a set of said data entry fields to a predetermined input value (Tran column 77, lines 33-47; column 779, lines 24-55; column 80, line 5 to column 81, line3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; Figure 40 Figure 44; and Figure 46);

iii. A second comparison circuit, said second comparison circuit operable to compare a first register address corresponding to a comparison match of said first comparison circuit to a second register address (Tran column 77, lines 33-47; column 779, lines 24-55; column 80, line 5 to column 81, line3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; Figure 40 Figure 44; and Figure 46); and

iv. A dispatch circuit operable to dispatch data of a second data entry field of a second register corresponding to said second register address to an operation unit in response to a decode of data in a third data entry field of said second register and a comparison match of said second comparison circuit (Tran column 106, line 35 to column 107, line 62; Figure 48; and Figure 49).

56. Tran has not taught a microprocessor comprising:

a. Random access memory (RAM);

b. Read only memory (ROM);

c. An I/O adapter; and

d. A bus system coupling devise internal to said CPU.

57. However, Tran has taught a microprocessor system (Tran Abstract, line 1 and column 1, line 19-22). Short has taught a microprocessor comprising:

a. Random access memory (RAM) (Short pages 12-13 and 72-76);

b. Read only memory (ROM) (Short pages 12-13 and 72-76);

c. An I/O adapter (Applicant's claim 10); and

d. A bus system coupling devise internal to said CPU (Short pages 12-13 and 72-76).

58. A person of ordinary skill in the art at the time the invention was made would have recognized that a typical computer system incorporates these elements, thereby ensuring that output data is produced, which is a specified function of an input data (Short page 72). Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the above elements of Short in the device of Rosenberg.

59. Referring to claim 27, Tran has taught wherein said operations are Load and Store operations within said processor (Tran column 77, lines 33-47; column 779, lines 24-55; column 80, line 5 to column 81, line3; Figure 38; Figure 39; and Figure 40).

60. Referring to claim 28, Tran has taught wherein said predetermined input value is a real address requesting particular data corresponding to one of a Load and a Store operation (Tran

column 77, lines 33-47; column 779, lines 24-55; column 80, line 5 to column 81, line3; Figure 38; Figure 39; and Figure 40).

61. Referring to claim 29, Tran has taught wherein said first scan comparison circuit comprises multiple like entry comparison circuits, each of said multiple like entry comparison circuits operable concurrently in parallel (Tran column 77, lines 33-47; column 779, lines 24-55; column 80, line 5 to column 81, line3; Figure 38; Figure 39; and Figure 40).

62. Referring to claim 30, Tran has taught wherein said operation unit comprises an Instruction Management Unit (IMU) (Trans column 6, line 52 to column 8, line 57 and Figure 1).

63. Referring to claim 31, Tran has taught wherein said operation unit comprises a Storage Management Unit (SMU) said SMU comprising data cache memory and controller and a Storage Reference Buffer (SRB) (Tran column 10, line 66 to column 11, line 15; column 77, lines 33-47; column 779, lines 24-55; column 80, line 5 to column 81, line3; Figure 1; Figure 38; Figure 39; and Figure 40).

64. Referring to claim 32, Tran has taught wherein one of said data entry fields is a Valid bit field, said Valid bit field indicating whether other data entry fields are valid (Applicant's claims 7 and 32) (Tran column 123, lines 2-15 and Figure 55).

65. Referring to claim 33, Tran has taught wherein one of said data entry fields is an Instruction Identification (ID) field corresponding to a particular Load and Store operation (Tran column 123, lines 2-15 and Figure 55).

66. Referring to claim 34, Tran has taught wherein one of said data entry fields is an Instruction status field corresponding to a status of one of said Load and Store operations (Tran column 123, lines 2-15 and Figure 55).

67. Referring to claim 35, Tran has taught wherein one of said data entry fields is a Load/Store field having a Load/Store bit, said Load/Store bit corresponding to a Load operation if said Load/Store bit has a first logic state and corresponding to a Store operation if said Load/Store bit has a second logic state (Tran column 123, lines 2-15 and Figure 55).

68. Referring to claim 36, Tran has taught wherein one of said data entry fields comprises Real Address field, said Real Address field corresponding to a particular Real Address of memory data (Tran column 123, lines 2-15 and Figure 55).

69. Referring to claim 37, Tran has taught wherein one of said data entry fields is a Quadword field, said Quadword field comprising multiple bytes of data (Tran column 123, lines 2-15 and Figure 55). In regards to Tran, he has taught the data is present in an entry field. The size of the field is not a patentable distinction.

70. Referring to claim 39, Tran has taught wherein said operation unit is a pipeline execution unit operating concurrently on a plurality of said data entry fields (Tran column 10, lines 17-55 and Figure 1).

71. Referring to claim 40, Tran has taught wherein said addressable registers are addressed using a plurality of address pointers (Tran column 77, lines 33-47; column 779, lines 24-55; column 80, line 5 to column 81, line3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; Figure 40 Figure 44; and Figure 46).

72. Referring to claim 41, Tran has taught wherein said addressable registers are configured as a Storage Reference Buffer (SRB) (Tran column 10, line 66 to column 11, line 15; column 77, lines 33-47; column 779, lines 24-55; column 80, line 5 to column 81, line3; Figure 1; Figure 38; Figure 39; and Figure 40).

73. Referring to claim 42, Tran has taught wherein one of said address pointers is a third pointer, said third pointer pointing to one of said addressable registers whose data entry fields contain data defining an earliest Store operation that is either unresolved or that matches a register address of a current Load operation (Tran column 70, lines 7-44 and Figure 36).

74. Referring to claim 43, Tran has taught wherein said address pointers comprise a fourth and a fifth pointer, said fourth and fifth pointers defining a window of register addresses from which a Load operation may be satisfied without having to access other memory storage (Tran column 70, lines 7-44 and Figure 36).

75. Referring to claim 44, Tran has taught wherein said second register address is selected from registers addresses which fall within a window of register addresses, said window of addresses defined by said address pointers (Tran column 70, lines 7-44; column 81, lines 1-3; and Figure 36).

76. Referring to claim 45, Tran has taught wherein one of said address pointers is a first pointer, said first pointer pointing to an IN register address of a first available register into which data may be added (Tran column 70, lines 7-44 and Figure 36).

77. Referring to claim 46, Tran has taught wherein one of said address pointers is a second pointer, said second pointer pointing to an OUT register address of a first available register from which register data may be retired (Tran column 70, lines 7-44 and Figure 36).

78. Referring to claim 47, Tran has taught wherein said data entry fields, added to said SRB after a mis-predicted branch instruction occurs in said processor, are retired and said first pointer is indexed to first register address of a register with added register data entry bits which were

added immediately prior to said mis-predicted branch instructions (Tran column 82, line 63 to column 83, line 22).

79. Referring to claim 48, Tran has taught wherein said window of register addresses defines active Load and Store operations (Applicant's claims 23 and 48) (Tran column 70, lines 7-44 and Figure 36).

80. Referring to claim 49, Tran has taught wherein said first pointer is indexed by one when said register data has been added, said first pointed having a minimum and a maximum value wherein a decrement down from a minimum value results in said maximum value and an increment up from said maximum value results in said minimum value (Tran column 70, lines 7-44 and Figure 36).

81. Referring to claim 50, Tran has taught wherein said second pointer is indexed by one when register entry bits have been deleted, said second pointer having a minimum and a maximum value wherein a decrement down from said minimum value results in said maximum value and an increment up from said maximum value results in said minimum value (Tran column 70, lines 7-44 and Figure 36).

82. Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tran et al., U.S. Patent Number 5,764,946 (herein referred to as Tran) in view of Kenneth L. Short's Microprocessors and Programmed Logic ©1981 (herein referred to as Short), as applied to claim 26 above, in view of Jerry M. Rosenberg's Dictionary of Computers, Information Processing & Telecommunications Second Edition ©1987 (herein referred to as Rosenberg). Tran has not explicitly taught wherein one of said data entry fields is an Operand Mask field, said Operand Mask field defining selected bytes of data within a selected one of said data entry fields.

However, Tran has taught miscellaneous control fields (Tran column 123, lines 2-15 and Figure 55). Rosenberg has explicitly taught a mask field (Rosenberg page 370). A person of ordinary skill in the art would have recognized that a mask field describes certain data needed 5while ignoring unnecessary data, thereby ensuring the unnecessary data does not affect the system. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the mask field of Rosenberg in the device of Tran.

Conclusion

83. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Reininger et al., U.S. Patent Number 5,539,892, has taught a cache connected to multiple comparators and a dispatch device.

b. Tran et al., U.S. Patent Number 5,761,712, has taught a load and store buffer.

c. Tran et al., U.S. Patent Number 5,765,035, has taught a cache with multiple comparators and dispatch device.

d. Ramagopal et al., U.S. Patent Number 5,802,588, has taught a load and store buffer.

e. Tran et al., U.S. Patent Number 5,761,712, has taught a load and store buffer.

f. Steiss et al., U.S. Patent Number 6,009,516, has taught a fetch unit connected to multiple comparators and a dispatcher.

g. Ramagopal et al., U.S. Patent Number 6,473,832, has taught a device which checks for cache dependencies.

84. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

85. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

86. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
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March 10, 2004

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